SCT ASIC PRR Document

SUMMARY OF IRRADIATION RESULTS

Abstract

This document summarises the irradiation results of the front-end ASIC - ABCD3TA.

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History of Changes

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1 SCOPE OF THE DOCUMENT

This document summarises the radiation test results of the front-end ASIC - ABCD3TA - to be used in the binary readout architecture of silicon strip detectors in the ATLAS Semiconductor Tracker (SCT). The ABCD3TA chip designed for the DMILL technology comprises in a single chip all functions required for the binary readout architecture. The DMILL technology is qualified as a radiation resistant one, however, the radiation levels expected for the SCT detector in the ATLAS experiments exceed the upper limits of those specified for the DMILL process, i.e. 100 kGy of the total ionising dose and 1×10^{14} n/cm^2 1 MeV eq. neutron fluence. In addition, if one takes into account very advanced requirements regarding the noise, speed and power consumption of the ABCD chip, it becomes obvious that radiation effects in the basic devices, although limited, can not be ignored.

The ABCD3TA design is the final version based upon the ABCD2T prototype chip, which was a major step in development of the front-end ASIC. All the prototypes, starting for the ABCD2T version, have been tested extensively for radiation hardness. The two recent steps in the development leading from the ABCD2T prototype to the ABCD3TA were driven by some particular the radiation effects. Most of the ABCD3TA design remains the same as in the ABCD2T prototype and in that sense the radiation test results obtain for the ABCD2T and ABCD3T versions remain valid for the ABCD3TA version and contribute to the overall statistics of irradiated chips.

Satisfactory matching of thresholds, a critical parameter for the binary architecture, has been achieved in the ABCD2T design by implementation of individual threshold correction in every channel using 4-bit digital-to-analogue converter (TrimDAC) per channel. Radiation tests showed that after proton irradiation up to a fluence of 3×10^{14} p/cm^{-2} the spread of the threshold offsets increased by a factor of 3 and exceeded the range of the TrimDACs. In order to not compromise the resolution of the TrimDAC, i.e. achievable uniformity of thresholds for non-irradiated chips, and to guarantee that for fully irradiated chips all the channels can be corrected, 4 selectable ranges of the TrimDAC have been implemented in the ABCD3T design.

Irradiation of the ABCD3T chips showed that the circuitry responsible for loading the range of the TrimDAC was not sufficiently robust and in some fraction of chips the required ranges could not be loaded correctly. A minor correction in the design, resulting in the ABCD3TA version, has been implemented after receiving two batches of the pre-production series. In the second part of the pre-production series the ABCD3TA version was manufactured. Radiation tests of the ABCD3TA chips have proved that the correction to the design is effective and the problematic block remains functional up to the nominal fluence of 3×10^{14} cm^{-2}.

2 RADIATION-HARDNESS REQUIREMENTS.

Radiation levels expected in the SCT detector are defined in the Atlas Inner Detector Technical Design Report. The design values for the front-end electronics are specified as (see ATLAS TDR 7, Table 11-12):

- Total Ionising Dose (TID) as 100 kGy
- Non-Ionising Energy Loss (NIEL) as 2×10^{14} n(1MeV eq.)/cm^2.

These numbers include simulation uncertainty of 50%.

For the Single Event Effects (SEE) the radiation levels have not been specified in the TDR. We have assumed conservatively that the fluence of hadrons with sufficient energy to trigger a SEE is the same as the fluence, which delivers the specified total value of NIEL

It is worth to note that these numbers are the maximum ones, which apply only to the most inner barrel and most outer disk of the SCT detector. For major part of the SCT these numbers are lower.

3 EXPECTED RADIATION EFFECTS IN THE ABCD3TA ASIC

There are two important aspects to be taken into account when considering the radiation hardness of the ABCD3TA design:

- the design is realised in a BiCMOS technology so one has to pay attention to the ionisation effects as well as to the displacement damages,
- there are a number of specific effects related to the ABCD3TA architecture and particular circuit implementations.

On top of a general requirement that the chip should be fully functional after irradiation up to the maximum specified levels, there are some particularly critical issues of the ABCD design, which should be considered carefully with respect to radiation effects. The most critical aspects are: noise of the front-end, matching in the front-end circuit, in particular the offset spread of the discriminator, and the speed of the digital CMOS part.

3.1 NOISE

The front-end circuit of the ABCD3TA chip is built as a transimpedance amplifier using a bipolar input transistor. One of the noise sources, which contribute to the equivalent input noise charge is the shot noise of the base current of the input transistor. Due to a short shaping time of 25 ns, as required for the SCT readout, and a large detector capacitance, the relative contribution of this noise is acceptable as long as the base current does not exceed a level about 2 μA. For given detector capacitance, shaping time and current gain factor β of the input transistor, one can find an optimum value for the collector current which yields a minimum value of ENC.

In modern bipolar transistors the current gain factor β is degraded by the ionisation effects as well as by the displacement damage. Both types of radiation effects, ionisation and displacement damage, lead to reduction of the lifetime of minority carriers in the transistor base. The ionisation effects lead to generation of recombination states at the interfaces $Si\text{-}SiO_2$ and consequently to recombination of minority carriers in the base periphery, while the displacement damages lead to generation of defects in the bulk and consequently to recombination of minority carriers in the base volume. Thus, a significant degradation of β has to be anticipated, which implies that first of all the circuit design has to be insensitive to variation of β, regarding DC bias conditions as well as AC characteristics. With respect to noise there are two issues to be taken into account, namely the size of the transistor and the collector current in the input transistor.

The degradation of β depends on the actual current density in the transistor, therefore from that point of view one would prefer to use a minimum geometry transistor in the input stage. On the other hand, in order to minimise the series noise contribution from the base spread resistance, one would rather use a large area input transistor. These two requirements are contradictory and an optimum size of the input transistors can be defined provided we know how the β degrades after irradiation for a given technology. The radiation effects in the bipolar transistors in the DMILL technology have been studied and based on these results we chose the emitter area of the input transistor to be $1.2\times10\ \mu m^2$.

We expect that β of the input transistor will change significantly, by a factor up to 4, during the lifetime of the ATLAS experiment. With the β value decreasing during the lifetime of the experiment the optimum value of the collector current in the input transistor will also decrease. In order to keep the series noise contribution at the acceptable level for the detector capacitance of 20 pF we cannot reduced the bias current in the input transistor below 150 μA. This limit defines the criteria for radiation resistance of the chips with respect to noise performance, namely, after full irradiation the whole front-end circuit must be biased correctly for the input transistor current of 150 μA and the parallel noise must be bellow 900 el. rms so that additional noise due to shot noise of the base current does not contribute significantly to the total noise. It is worth to note that there are other effects, as increase of the detector leakage current and increase of the interstrip capacitance, which contribute to the noise of a fully irradiated module.

In order to be able to adjust the current in the input transistors and optimise the noise performance according to the actual value of β we have implemented a 5-bit DAC to control this current. In addition, the bias current in the following stages of the front-end amplifier is also controlled by another 5-bit DAC, which allows to adjust DC biasing of the circuit and compensate the drifts due to decrease of β in

the bipolar transistors, shifts of the threshold voltages in MOS transistors and increase of resistor values.

3.2 THRESHOLD MATCHING

One of the most critical issues of the binary architecture, as implemented in the ABCD design, is the matching of parameters of the front-end circuit since a common threshold for 128 channels in one chip is used. The effective threshold of the discriminator is determined by the offset of the discriminator and by the gain of the amplifying stages preceding the discriminator. The preamplifier stage has to be implemented in a single-ended configuration and the gain of the circuit is sensitive to variation of resistors which are used in the feedback loops. Thus, channel-to-channel matching of the gain is limited by the resistor matching across the whole chip. The discriminator circuit is based on a fully differential structure so that the offset of the discriminator is determined by the local matching of resistors and transistors. From the tests performed for the ABCD prototype we have concluded that:

- matching of resistors is a limiting factor for the offset spread in the discriminator,
- matching performance of resistors, which are available in the DMILL technology, is not sufficient to guarantee that the SCT requirements regarding the threshold spread can be met using the original scheme of the discriminator,
- matching of resistors degrades significantly after irradiation.

In order to guarantee the required matching of threshold we have implemented in the ABCD3TA design individual threshold correction per channel (TrimDACs). In order to guarantee that for fully irradiated chips all the channels can be corrected, 4 selectable ranges of the TrimDAC have been implemented in the ABCD3T design.

Radiation hardness acceptance criteria with respect to the offset spread is defined by the maximum range of the TrimDAC, i.e. 240 mV. This means that after full irradiation the peak-to-peak offset spread must be less than 240 mV, which translates for the rms value of the offset spread to be less than 40 mV, assuming that the offset spread within one chip has statistical distribution.

3.3 SPEED OF DIGITAL CMOS BLOCKS

The digital part of the ABCD3TA chip comprises a number of various blocks, including static and dynamic logic, synchronous and asynchronous circuits. The chip is required to work at a clock frequency of 40 MHz for any set of corner parameters as specified by the vendor, including the changes after irradiation up to 100 kGy. In addition, the ABCD3TA chip is designed for a digital power supply of 4 V, which is below the nominal supply voltage of 5 V specified for the DMILL technology. In order to cover possible variation of the process parameters, temperature, supply voltage and post-radiation changes, the digital part of the ABCD chip was designed to work at least at a clock frequency of 80 MHz for the typical process parameters before irradiation and for supply voltage of 4 V. The main expected radiation effect is degradation of maximum speed

4 IRRADIATIONS

Irradiation of the ABCD chips have been performed in four different radiation environments due to combination of test requirements and availability of radiation sources:

- 24 GeV/c proton beam from the PS accelerator at Cern,
- neutrons from nuclear reactor at Ljubljana,
- pion beam at PSI,
- X-ray source.

4.1 PROTON IRRADIATION

4.1.1 IRRADIATION FACILITY

The 24 GeV/c proton beam delivered from the PS accelerator serves as the basic radiation source for irradiating SCT components and it is used as a standard test bed. It provides radiation environment similar to what is expected in the ATLAS experiment. From the point of view of radiation effects in electronics it allows to test at the same time all three aspects: Total Ionising Dose (TID), Non-Ionising Energy Loss (NIEL) and Single Event Effects (SEE). It covers also possible combinations of all three aspects which may be missed when performing dedicated tests in the radiation environments where one of the three aspects dominates, like neutron irradiation for study the NIEL, or X-ray irradiation for study TID.

The PS facility allows to irradiate ASICs in the conditions, which are as close as possible to the conditions expected in the experiment. The ASIC have been irradiated either on prototype hybrids being developed for the SCT silicon strip modules or on full SCT modules, including silicon strip detectors. During irradiation the ASICs were biased, clocked and read out all the time so that all the blocks were exercised in the same way as in the experiment. The SCT readout system based on VME modules, CLOAC, MuSTARD and SLOG was used for pre-irradiation and post-irradiation chip testing as well as for controlling the chips during irradiation. It is important to note that on the hybrid/modules the chips were used in the same electrical configuration as they will be used in the experiment. In particular, this configuration allows to test the functionality and performance of token data path including 6 or 12 chips as well as the redundancy scheme. This is an important issue as correct operation of the data token path is the most sensitive to degradation of timing performance of the digital part.

For majority of irradiated chips they were kept at low temperature below 0 deg as this was driven by cooling requirements for the silicon strip detectors.

The only aspect which was different in the irradiation experiments compared to the ATLAS experiment was the dose rate. At the PS facility the nominal SCT fluence of 3×10^{14} p/cm^{-2} is usually delivered within a period 6-10 days, resulting in relatively high dose rate. In all irradiation full fluence of 3×10^{14} p/cm^{-2} has been delivered to ASICs. This fluence is equivalent to 100 kGy of TID, 2×10^{14} n/cm^{-2} with respect to NIEL and 3×10^{14} p/cm^{-2} with respect to SEE.

Details on the PS irradiation facility can be found at:

http://atlas-sct-irradiation.web.cern.ch/atlas-sct-irradiation/default.htm

4.1.2 INVENTORY OF ABCD CHIPS IRRADIATED AT PS

Table 4.1: Summary of proton irradiation.

Irradiation session	**Version of ABCD**	**Irradiated object (number of chips)**	**Fluence**	**Test goals ***
Apr 2000	ABCD2T	module (12 chips)	3×10^{14} p/cm^{-2}	F, A, D, P, S
		hybrid (6 chips)	3×10^{14} p/cm^{-2}	
Aug 2000	ABCD2T	hybrid (6 chips)	3×10^{14} p/cm^{-2}	F, A, D, P, S
	ABCD3T	hybrid (6 chips)	3×10^{14} p/cm^{-2}	
Oct 2000	ABCD3T	module (12 chips)	3×10^{14} p/cm^{-2}	F, A, D, P, S
	ABCD3T	module (12 chips)	3×10^{14} p/cm^{-2}	
	ABCD3T	module (12 chips)	3×10^{14} p/cm^{-2}	
	ABCD3T	hybrid (12 chips)	3×10^{14} p/cm^{-2}	
Nov 2000	ABCD3T	module (12 chips)	3×10^{14} cm^{-2}	F, A, D, P
Apr 2001	ABCD3TA	module (12 chips)	3×10^{14} p/cm^{-2}	F, A, D, P
		module (12 chips)	3×10^{14} p/cm^{-2}	
		hybrid (12 chips)	3×10^{14} p/cm^{-2}	
		hybrid (12 chips)	3×10^{14} p/cm^{-2}	
May 2001	ABCD3TA	module (12 chips)	3×10^{14} p/cm^{-2}	F, A, D, P
		module (12 chips)	3×10^{14} p/cm^{-2}	
		hybrid (12 chips)	3×10^{14} p/cm^{-2}	

*Test goals: F - functionality
A - analogue performance
D - digital performance
P - power
S - Single Event Effect

Total numbers of irradiated chips: ABCD2T 24
ABCD3T 64
ABCD3TA 84

4.1.3 TEST PROCEDURES

The test procedures used for characterisation of chips are the same as those used for QA characterisation of hybrids and modules. Typical sequence of pre-irradiation, in-situ and post-irradiation characterisation of each chip on the hybrid/module is described below.

4.1.3.1 PRE-IRADIATION MEASUREMENTS

Full characterisation of chips include five group of measurements:

A) The module QA characterisation procedure, but with full trimming of all four trim ranges, for the nominal bias conditions of the front-end. The tests are described in the Electrical Tests document http://hepwww.rl.ac.uk/atlas-sct/documents/Electrical_Tests.htm

The full characterisation sequence include:

- Power On test
- Standard/Redundant Clock/Command reception test
- Full Bypass Functionality Test at several digital supply voltages from 3.3 V to 5.0 V in steps of 0.1 V

- Pipeline Efficiency Scan
- Strobe Delay Scan
- Three Point Response Curve
- TrimScan – response curves of TrimDACs for all four TrimRanges
- Full Response Curve
- Noise Occupancy Scan
- Time Walk.

B) Reduced Response Curves for four values of the input charge Qin = {1, 2, 3, 4} fC are measured for a set of preamplifier and shaper current settings given by matrix of the two currents.

Ipre = {100, 150, 200, 250} μA

Ishpr = {20, 30} μA

C) Pulse Shape for charges 2 and 3 fC. Threshold scan for each charge and every forth strobe delay value gives pulse shape, gain and noise as a function of strobe delay.

D) Speed of the Strobe Delay circuitry. As this circuit is built as a chain of inverters, measuring number of strobe delay counts per one clock period of 25 ns gives a direct measure of speed of the CMOS transistors. This is measured as a function of digital supply voltage over the range 3.3 V to 5.0 V in steps of 0.1V.

E) Power Characteristics.

Digital current Idd vs. Vdd

Analogue current Icc vs. Vcc

Analogue current Icc vs Ipre/Ishpr

4.1.3.2 IN-SITU MEASUREMENTS

During irradiation a reduced set of measurements is performed in-situ at the fluences: 0, 0.5, 1.0, 1.5, 2.0, 2.5 and 3.0×10^{14} p/cm^2, or at some subset of these fluences, depending on the fluence rate delivered from the accelerator and time constraints due to other material being irradiated at the same time. These measurements allowed to monitor degradation of parameters with accumulated fluence. Initially, the currents Ipre/Ishpr in the front-end circuit were set to 220 μA /30 μA but from 1.0×10^{14} p/cm^2, the FE settings were 150 μA /20 μA. Typical set of in-situ measurements include:

A) Full Bypass Functionality Test at several digital supply voltages from 3.3 V to 5.0 V in steps of 0.1 V.

B) Speed of the Strobe Delay circuitry as a function of digital supply voltage from 3.6 V to 5.0 V in steps of 0.2 V.

C) Strobe Delay Scan.

D) TrimScan (all four TrimRanges, 16 DAC values).

E) Three point RC (Qin = 1.5, 2, 2.5 fC).

F) Reduced Response Curves for three values of the input charge Qin = {2, 3, 4} fC are measured for a set of preamplifier and shaper current settings given by matrix of the two currents:

Ipre = {100, 150, 200} μA

Ishpr = {20} μA

G) Pulse Shape for charges 2 and 3 fC.

H) Power Characteristics.

Digital current Idd vs. Vdd

Analogue current Icc vs. Vcc

4.1.3.3 POST-IRRADIATION MEASUREMENTS

A) Reduced response curve for three values of the input charge Qin = { 2, 3, 4} fC for a set of preamplifier and shaper current settings. Due to degradation of the current gain factor β in bipolar transistor used in the front-end circuit it is expected that the optimum setting of the bias currents Ipre/Ishpr will change after irradiation. This is the initial step to determine the optimal current settings for each chip, and must be done before any further analogue measurements are performed. A range of scans, to find the optimal operation point is:

Ipre = {101.2, 119.6, 138, 156.4, 174.8} μA

Ishpr = {18, 24, 30} μA

B) The module QA characterisation procedure, but with full trimming of all 4 trim ranges. The tests are described in the Electrical Tests document, and the procedure consists of:

- Power On test
- Standard/Redundant Clock/Command reception test
- Full Bypass Functionality Test at several digital supply voltages from 3.3 V to 5.0 V in steps of 0.1 V
- Pipeline Efficiency Scan
- Strobe Delay Scan
- Three Point Response Curve
- TrimScan – response curves of TrimDACs for all four TrimRanges
- Full Response Curve
- Noise Occupancy Scan
- Time Walk.

C) Pulse Shape for Charges 2 and 3 fC.

D) Strobe Delay Circuitry Speed as a function of digital supply voltage from 3.3V to 5.0V in steps of 0.1 V.

E) Power Characteristics.

Digital current Idd vs. Vdd.

Analogue current Icc vs. Vcc.

Analogue current Icc vs Ipre/Ishpr.

4.1.3.4 SINGLE EVENT EFFECT MEASUREMENT

Since the ABCD3TA chips will be exposed in the experiment mainly to high energy charged particles and neutrons single event effects (SEE) are equally important as the total dose effects. Given the architecture of the ABCD3TA chip there are two major types of digital blocks which may be affected by SEE, namely the pipeline and the static registers which contain information about chip configuration and settings of operating points.

Irradiations at the PS accelerator were used to evaluate sensitivity of the ABCD3TA ASIC to Single Event Effects. The PS accelerator has a super-cycle of 14.4 s (or 19.2 s). During this super-cycle the T7 beam line receives between one and three spills of particles, each lasting 400 ms and containing in the order of 10^{10} particles.

For evaluation of the sensitivity of the ABCD design on SEE we have selected two different blocks, for which we could identify errors caused by single bit-flips, namely the mask register and the pipeline. The mask register design is based on static logic cells which are used in other registers in the chip: configuration register and DAC registers. The pipeline is based on dynamic cells which are used only in this particular block.

In order to measure SEE a dedicated data acquisition program was run during irradiation, which allowed to estimate the rate of SEE in particular digital blocks of the ABCD3TA chip. The

measurements were done using the Test Mode, in which test vectors were supplied to the input register and subsequently read out through the entire data path.

The following procedure is triggered by the beam signal from PS, marking the start of each spill:

- Load the mask register with zeros
- Send soft reset (as a precaution)
- Wait 140 clock cycles to make sure that the pipeline is filled with data from the mask register
- Set accumulator mode (write configuration register, which puts the chip in Send ID)
- Send soft reset, to clean the accumulator register
- Read mask register (send L1), as an reference to compare with pattern after spill
- Set accumulator mode (write configuration register, which puts the chip in Send ID)
- Read configuration register (send L1). Repeat once more to be sure that a bit-flip actually comes from a SEU and not from a transmission error
- Wait until the spill is over, typically 400ms
- Read configuration register (send L1), repeat once
- Set Data Taking Mode
- Read accumulator register (send L1), repeat once
- Reset Accumulator mode (write configuration register, which puts the chip in Send ID)
- Set Data Taking Mode,
- Read mask register (send L1), repeat once.

Interpretation of data is as follows:

A '1' read out from the accumulator register indicates that a bit-flip has occurred either in the mask register or in the pipeline sometime during the spill.

A '1' read out from the mask register indicates a bit-flip in the mask register.

A bit-flip is considered to be SEE if it is present in both the two after-spill measurements but not in the pre-spill measurement.

In order to confirm that the observed bit-flips are due to SEE the occurrence of bit-flips were correlated with the position of beam on given chips and the measurements were repeated in the periods between the spills.

4.1.4 TEST RESULTS

4.1.4.1 FUNCTIONALITY

Given extreme radiation levels to which ABCD3TA ASICs will be exposed in the experiment it is expected that their performance will be deteriorated by radiation effects. Our goal was to design the chip in such a way to leave some room for deterioration of performance so that after 10 years of operation of the experiment the chips will meet basic requirements. As the ABCD3TA ASIC is a complex mixed-mode design a first requirement is that all the block remain fully functional and the chips can perform all necessary operations in the data taking mode, as well as all the diagnostic functions remain fully operational.

In the ABCD2T chips excessive leakage current in the digital part was observed after irradiation. In the initial irradiation experiments of ABCD2T chips we faced a problem that this excessive current caused to much voltage drops on the digital power supply long cables and we could not read out the chips correctly in the irradiation area. The source of this excessive current has been traced down to a particular latch structure, which was used in various block of the chip. The design has been corrected in the ABCD3T version.

A functionality problem occurred in the ABCD3T version, namely after full irradiation the ranges of the TrimDAC could not be set correctly. The source of the problem has been identified as not sufficient buffering of signals to write the memory cells responsible for setting the TrimDAC range. The design

has been corrected successfully in the ABCD3TA version and the problem has not occurred in any of the 84 ABCD3TA chips irradiated.

Another functionality problem, which occurred in about 20% of irradiated ABCD3T chips, was corruption of data in the token data path in the nominal digital power supply range (3.8 - 4.2 V). Correct functionality of all chips showing this problem could be recovered by increasing the supply voltage up to 4.5 - 4.8 V, depending on the chip. The source of the problem has been identified as in the receiver circuit in the token path, however, one should keep in mind that:

- the problem occurred only in about 20% of irradiated ABCD3T chips,
- all chips which developed the problem came from one particular wafer,
- this particular wafer came from a lot which was not qualified by vendor for radiation resistance (irradiation was not performed because time constraints)
- the problem could not be reproduced in simulation assuming degradation of device parameters as specified by vendor, even more, the problem could not be reproduced assuming degradation of parameters by factor of 2 larger than expected for the worst case post-rad corner.

As none of the 84 irradiated ABCD3TA chip showed this problem, dropping the percentage of ABCD3T+ABCD3TA chips with the problem to less than 10%, and as the problem manifested itself only after half the full fluence spec (roughly 8 years of ATLAS running), we believe that the probability of this problem causing a problem in the SCT is very small. We have good reasons to expect that it will be never repeated for correctly qualified lots.

4.1.4.2 ANALOGUE PERFORMANCE

The ABCD3TA is required to guarantee after full dose irradiation analogue performance which are required for efficient operation of the overall SCT detector. The critical analogue parameters, which impact the detector efficiency and off detector readout electronics are: noise, threshold uniformity, time walk.

The analogue performance of fully irradiated modules to a fluence of 3×10^{14} p/cm^{-2} is presented in the document: "SCT Barrel Module: Electrical Performance". The results demonstrate that the fully irradiated modules built of ABCD3TA chips maintain full functionality and satisfactory noise and threshold spread as required for the SCT detector.

Here we present additional measurements, which demonstrate that analogue parameters behave after irradiation as expected and assumed in the design. As discussed before, we expect the current gain factor β to be reduced after irradiation and consequently the base current of the input transistor to increase for the collector current kept at constant value. Plot in Fig. 4.1. illustrates the equivalent input noise measured for the chips without silicon strips connected to the inputs as a function of proton fluence. Each curve represents the average for 128 channels in one chip. In such configuration the total capacitance at inputs of preamplifier is negligible and the ENC is dominated by the parallel noise due to shot noise of the base current. The measured increase of noise is consistent with expected decrease of β and with the expected increase of ENC assumed in the TDR (see ATLAS TDR 7, sec. 11.4.4.2).

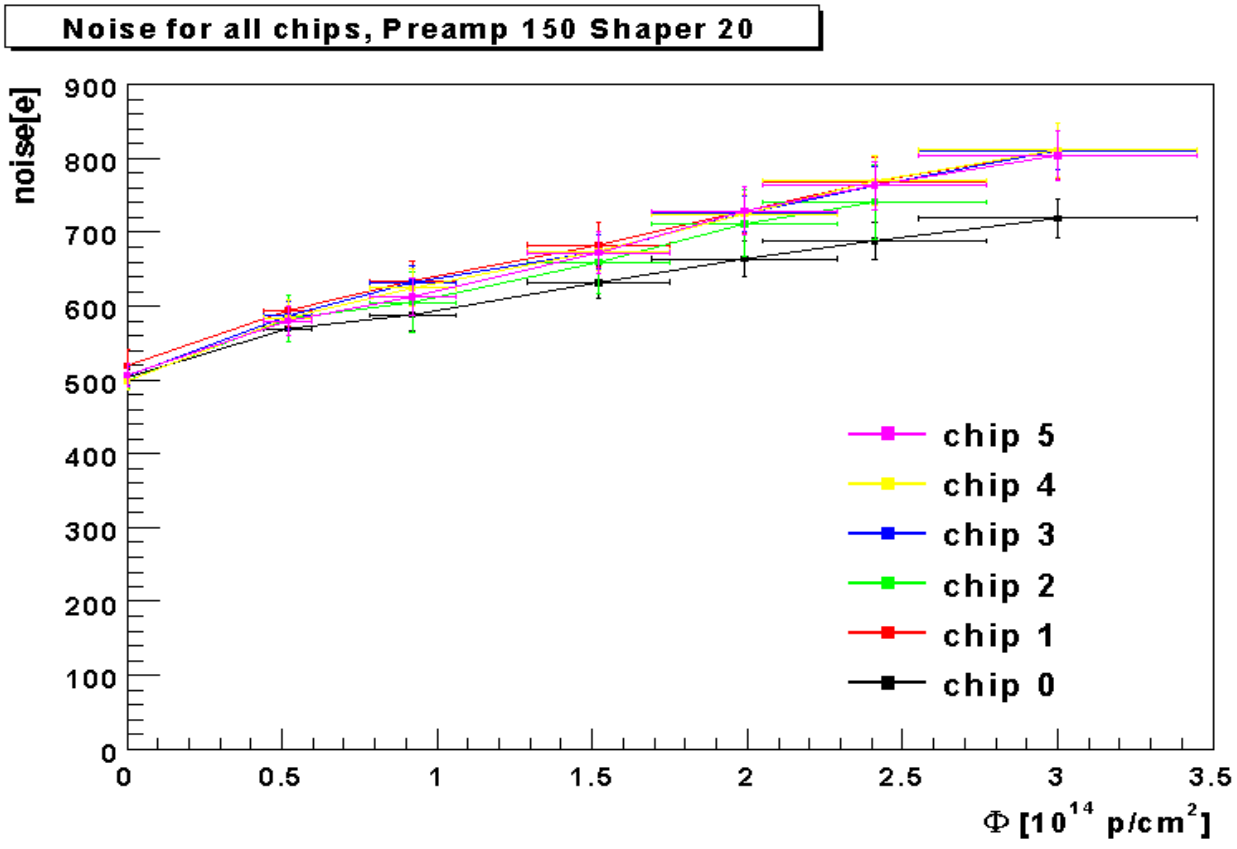

Figure 4.1: Parallel noise as a function of proton fluence.

Another effect, which was not expected from the beginning of the project but has been observed systematically in all irradiated prototypes, is an increase of the offset spread in the discriminator. The source of this effect has been identified as worsening of resistor matching. This effect has led us eventually to the ABCD3TA design with individual threshold correction per channel and with selectable four ranges of the TrimDACs. The evolution of the offset spread vs. proton fluence for 6 irradiated ABCD3T chips is shown in Fig. 4.2. Effectiveness of the TrimDACs has been demonstrated in trimming of fully irradiated modules, as shown in the document "SCT Barrel Module: Electrical Performance".

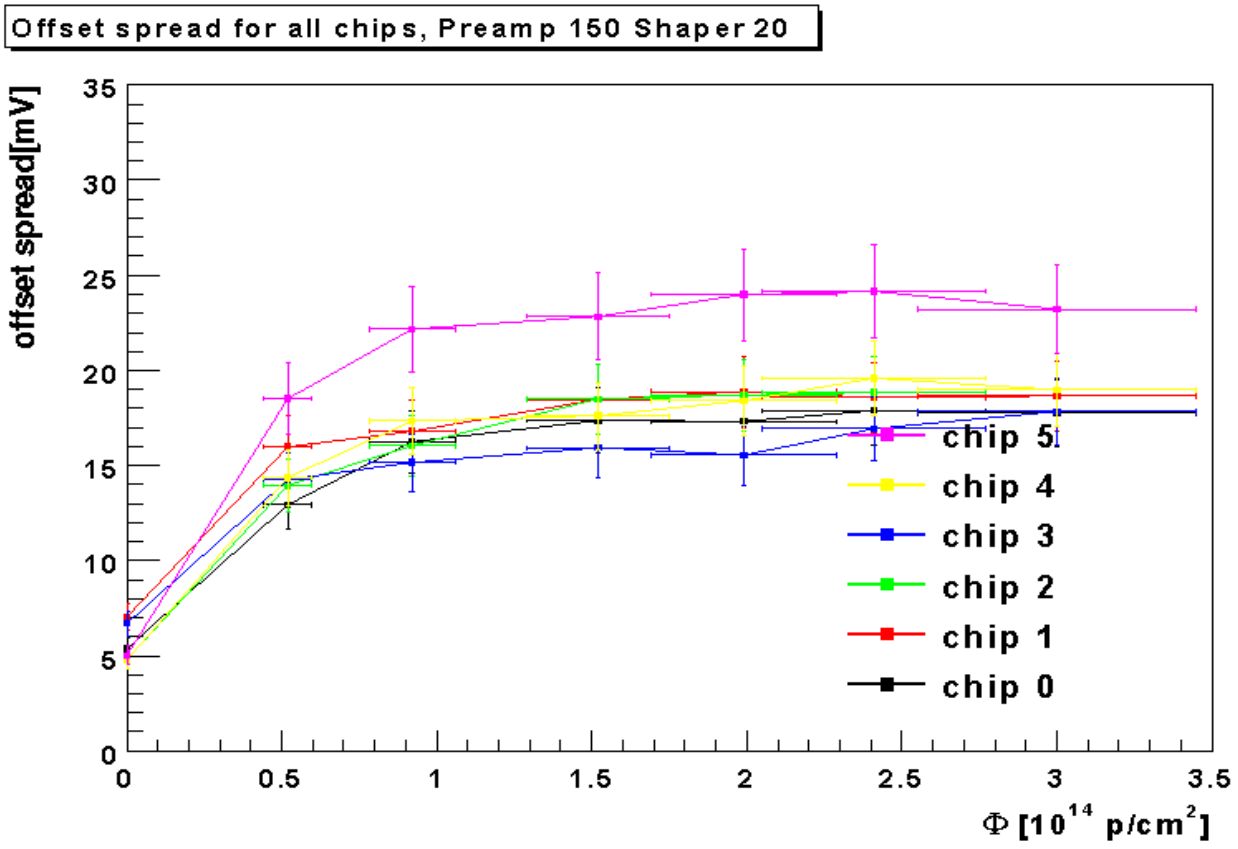

Figure 4.2: Evolution of the offset spread as a function of proton fluence.

It is worth to note that the results concerning behaviour of the two critical parameters, parallel noise and offset spread, is very consistent for all irradiated chips and it does not show any difference between the versions ABCD2T, ABCD3T and ABCD3TA.

4.1.4.3 SINGLE EVENT EFFECTS

An example of SEE data is shown in Fig. 4.3. The plot shows the number of SEE counted in the pipeline of one chip while the beam was scanned across the hybrid with 6 ABCD2T chips. The upper plot shows the SEE counts performed within the beam spills and the lower plot shows the SEE counts outside the beam spills.

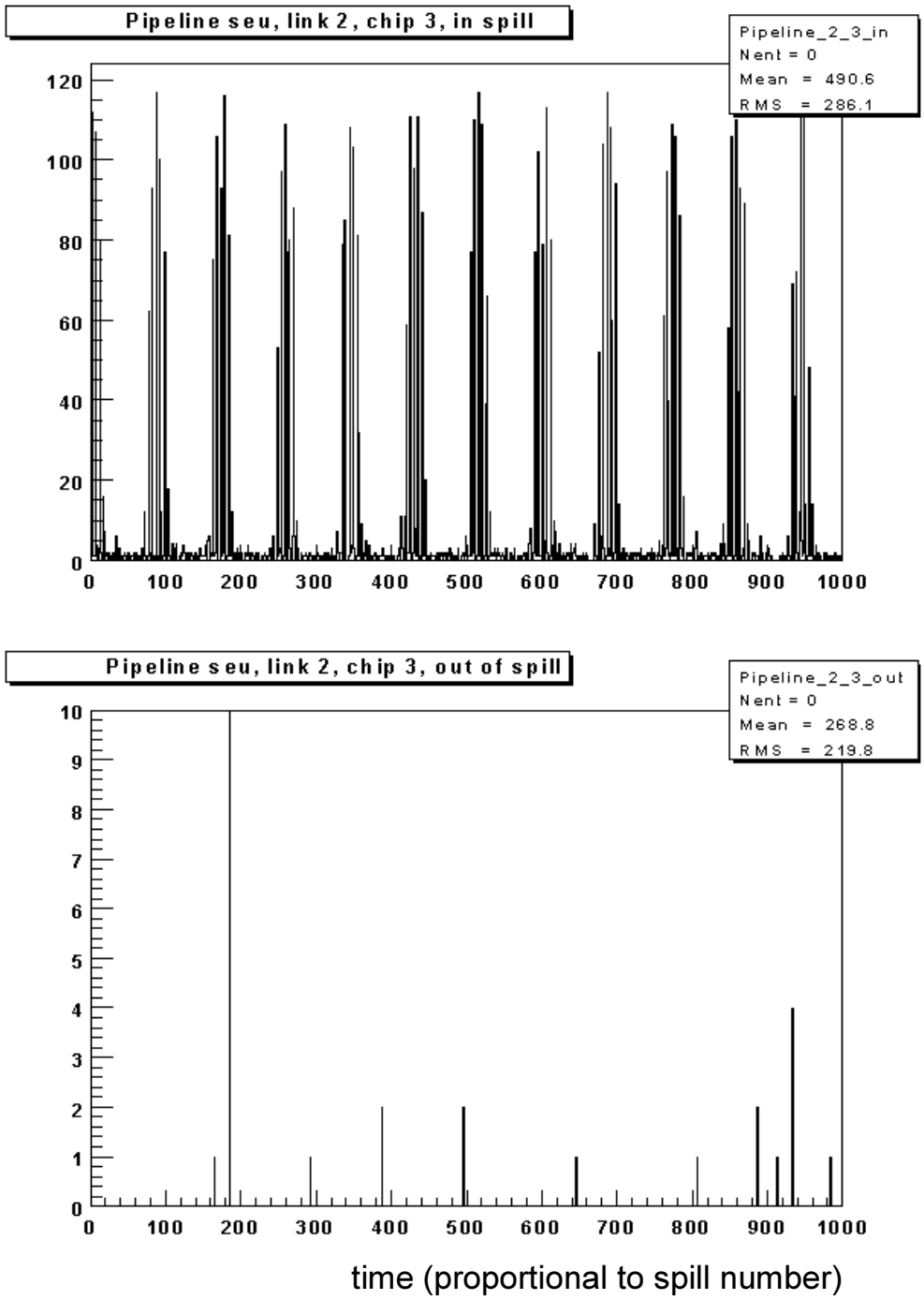

Figure 4.3: Measurement of SEE in the pipeline during proton irradiation.

Typical sensitivity to SEE for the two different types of memory cells measured in the 24 GeV/c proton beam is shown in Table 4.2. As one can expects the sensitivity of the pipeline is much higher, about 50 times compared to the sensitivity of static registers, like the mask register.

Table 4.2: SEE sensitivity of the pipeline and the mask register measured in 24 GeV/c proton beam at PS.

Chip position on hybrid	M0	S1	S2	S3	S4	E5	
SEE in pipeline	1.24	1.08	1.08	1.10	1.08	1.10	$\times 10^{12}$/p/cm^2/flip
SEE in static registers	5.00	4.07	4.00	4.24	4.70	5.28	$\times 10^{13}$/p/cm^2/flip

Any bit flip in the pipeline causes a single data error and the rate of such events should be compared with the noise rate expected from the front-end circuit. Such errors will not require any intervention. Assuming that the full fluence of 3×10^{14} p/cm^2 corresponds to experiment run time of 1×10^{8} s at high luminosity one can expect a SEE rate of 3×10^{-6}/bit/s. Thus, SEE rate per channel (132 bits in the pipeline) and per collision is given as: 3×10^{-6}/bit/s × 132 bits / 4 × 10^{7} /s = 1×10^{-11}. This number in negligible when compared with the expected noise occupancy on the order of 1×10^{-4}.

All static registers in the chips, like configuration registers, DAC registers, strobe delay register, are built of the same cells as the mask register. Measurements of the SEE sensitivity were performed for the mask register as the ABCD architecture allows for unique identification of errors which occur in this register. Then we assume the SEE sensitivity of other static registers in the chip is similar as the sensitivity of the mask register.

The errors in static registers may lead to changes of static biases in the front-end, setting of the threshold or changes of operation mode. In order to recover from such errors it will be needed to reload the chip configuration. From our measurements we obtain SEE rate in static registers about 6×10^{-8}/bit/s. In the configuration register we have 10 critical bits per chip which when flipped may corrupt the data stream. As 6 ABCD3TA chips are read out via one optical link we have to take into account 60 bits and we obtain a rate 3.6×10^{-6}/link/s. A bit flip in one of the DACs (threshold, preamplifier current, shaper current, TrimDAC) may lead to a change of setting. In total there is 530 bits, including 512 bits of the TrimDACs. This gives the SSE rate of 3.25×10^{-5}/chip/s. These bits are not as critical for the chip operation as the bits in the configuration register. In most cases bit flips in these registers will lead to a non-optimum setting of the operation conditions but the chips will remain operational.

In order to recover from the errors in the static registers it will be necessary to reset periodically the front-end electronics and re-load the configuration files. From the estimated above SEE sensitivity of the configuration register one can expect a mean time of fault-free operation to be about 2.8×10^{5} s for each data link (6 chips) at high luminosity.

4.2 NEUTRON IRRADIATION

Neutron irradiation has been performed in order to test the ABCD3TA chips with respect to the NIEL effects. This irradiation served as a crosscheck of the NIEL effects observed in proton irradiation.

Irradiation was done in the core of the TRIGA nuclear reactor in the Jozef Stefan Institute at Ljubljana. The chips were irradiated on the hybrids using a similar electrical scheme as in the proton irradiation at PS. The chips were biased, clocked and read out during irradiation. The chips were irradiated up to the nominal fluence of 2.0×10^{14} n(1 MeV eq.)/cm^2. The irradiation were done in four steps with characterisation of chips at fluences: 0, 0.5, 1.0, 1.5, 2.0×10^{14} n/cm^2. The characterisation of chips was focused on measuring the analogue performance since we do not expect any affect of neutron irradiation on the CMOS circuitry. At each step the response curve were measured for matrix of the bias current in the front-end circuit according to similar procedures as described in sec. 4.1.3.

4.2.1 INVENTORY OF ABCD CHIPS IRRADIATE WITH NEUTRONS

Table 4.3: Summary of neutron irradiation

Irradiation session	**Version of ABCD (production lot)**	**Irradiated object (number of chips)**	**Fluence**	**Test goals***
Oct 1999	ABCD2T	hybrid (3 chips)	2×10^{14} n/cm^{-2}	F, A
Dec 1999	ABCD2T	hybrid (6 chips)	2×10^{14} n/cm^{-2}	F, A
Mar 2001	ABCD3T	hybrid (12 chips)	2×10^{14} cn/m^{-2}	F, A

*Test goals: F - functionality

A - analogue performance

Total numbers of irradiated chips: ABCD2T 9

ABCD3T 12

In addition some numebr of test structures, containg bipolar transistor and resistors, have been irradiated in the TRIGA reactor in Ljubjana and in the Prospero facility.

4.2.2 TEST RESULTS

4.2.2.1 FUNCTIONALITY

In neutron irradiation the question about functionality applies only to the front-end part. Large degradation of the current gain β in the bipolar transistors and changes of resistor values may potentially lead do such large shift of the DC operating points that the front-end circuit is not operational any more. All irradiated chips can be correctly biased after receiving the full fluence. Adjustment of bias currents in the front-end circuit (preamplifier current and shaper current) is required to maintain correct bias and to optimise the noise performance.

4.2.2.2 ANALOGUE PERFORMANCE

The two critical analogue parameters, noise and offset spread, have been measured for all irradiated chips. Typical plot of parallel noise vs fluence is shown in Fig. 4.4. One can notice that the noise level after neutron fluence of 2×10^{14} n/cm^{-2} is within statistical fluctuations the same as the noise level after proton irradiation to a fluence of 3×10^{14} p/cm^{-2}. Given that the two irradiations correspond to the same value of NIEL and that the parallel noise is determined by the current gain factor β in bipolar transistors one can draw a conclusions that in the proton irradiation the degradation of β is mainly due to the NIEL.

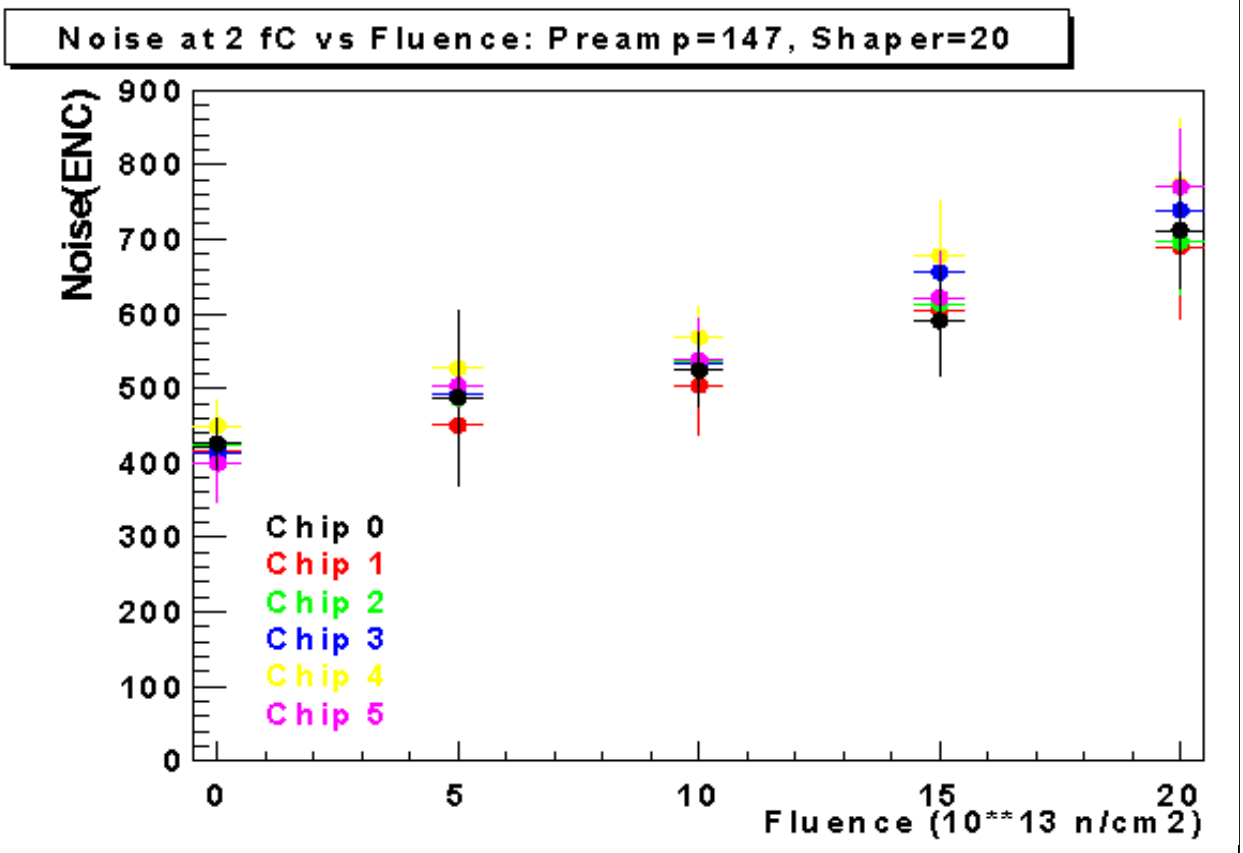

Figure 4.4: Parallel noise as a function of neutron fluence.

The evolution of the offset spread as a function of neutron fluence is shown in Fig. 4.5. The offset spread increases rapidly at the beginning of irradiation and then saturates, similarly as in proton irradiation. The offset spread increases after neutron irradiation by a factor about 2, while after proton irradiation it increases by a factor 3-4. This increased offset spread is covered well by the maximum range of the TrimDACs.

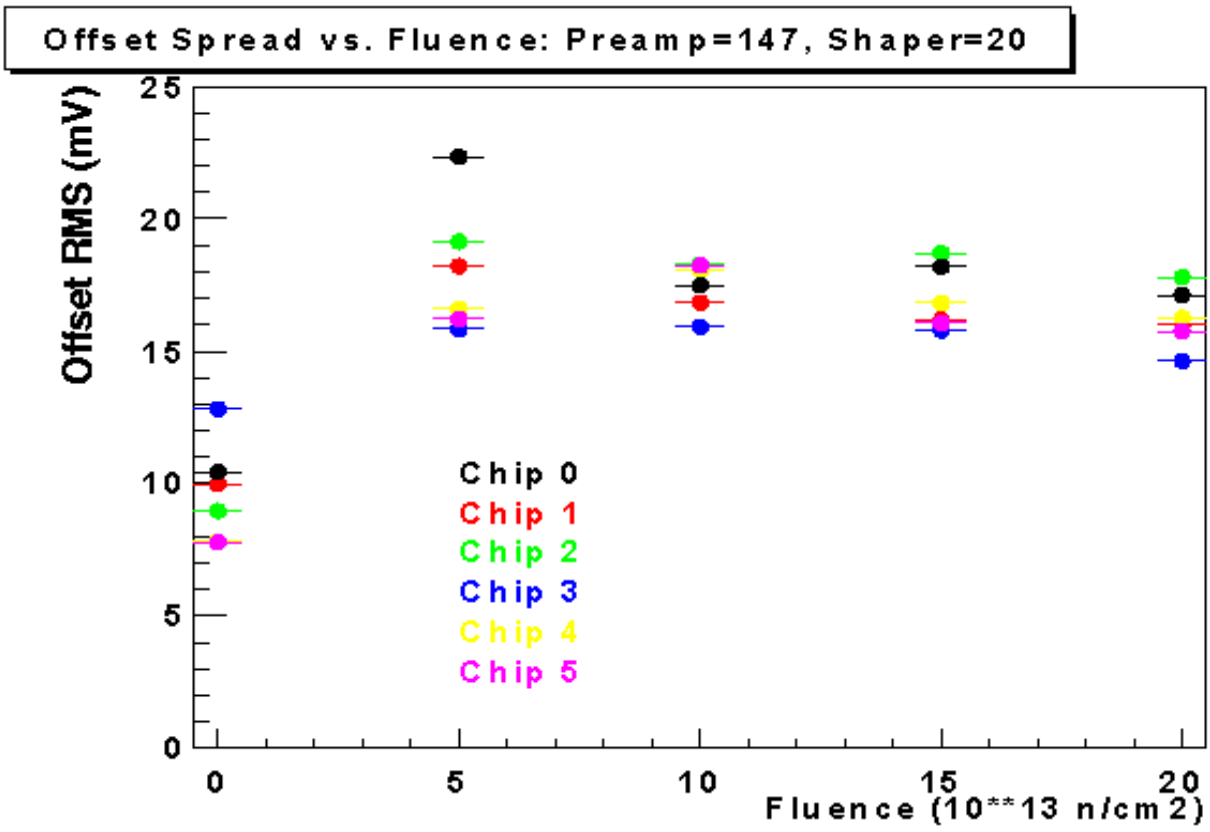

Figure 4.5: Evolution of the offset spread as a function of neutron fluence.

Due to limited space in the reactor tube there is impossible to irradiate full SCT modules as it is done in the proton beam at PS. Regarding the noise in a full module, in addition to the parallel noise measured on for the chips irradiated on the hybrids, there will be contribution form the series noise, which depends only on the bias current in the input transistor and is be proportional to the total strip capacitance. Since after neutron irradiation we observe the parallel noise not higher the after proton irradiation for the same bias current we can conclude that the noise of a full module will not be higher than this observed in proton irradiation, providing the radiation damages to detectors will be similar.

The offset spread is an internal feature of the ABCD3TA design and does not depend on the on the capacitive load at the inputs of front-end circuits. Thus, we expect to see the same offset spread for full modules as we observe for the irradiated hybrids.

4.3 PION IRRADIATION

A high-energy pion beam offers the radiation environment closest to the one expected in the ATLAS experiment, however, availability of this is limited. Therefore only limited number of tests have been performed in the pion beam with a main goal to verify that there are no unexpected NIEL effects in the pion irradiation compared to the proton irradiation and to cross check the PS SEE measurements in a beam of different time structure and different energy of particles.

A hybrid with 6 ABCD2T chips have been irradiated in the 200 MeV/c pion beam at PSI. Because of the constraints in the beam area the hybrid was not irradiated uniformly and the chips receive fluences between 1.00×10^{14} π/cm^2 and 2.24×10^{14} π/cm^2. The irradiation experiment was performed in a similar way as all the proton irradiations. In particular, the readout system used and the measurement program were the same as used in all proton irradiations. The SEE sensitivity was measured as well.

4.3.1 INVENTORY OF ABCD CHIPS IRRADIATE WITH PIONS

Table 4.4: Summary of pion irradiation.

Irradiation session	**Version of ABCD**	**Irradiated object (number of chips)**	**Fluence**	**Test goals***
Jul 2000	ABCD2T	hybrid (6 chips)	1.0×10^{14} π/cm^{-2} - 2.24×10^{14} π/cm^{-2}	F, A, S

*Test goals: F - functionality
A - analogue performance
S - Single Event Effect

Total numbers of irradiated chips: ABCD2T 6

4.3.2 TEST RESULTS

4.3.2.1 FUNCTIONALITY

All irradiated chips remained fully functional after receiving the full fluence.

4.3.2.2 ANALOGUE PERFORMANCE

It should be noted that pion irradiation have been performed on the ABCD2T version chips. However, the front-end design, except adding the TrimDACs, is identical in the ABCD2T and the final ABCD3TA version. There're, the test results with respect to analogue performance of the front-end obtained for the ABCD2T chips remains valid for the ABCT3TA chips.

Given the amount of NIEL and TID received by chips during pion irradiation we expect the degradation of the critical analogue parameters, parallel noise and offset spread, to be similar as in proton irradiations. The parallel noise as a function of pion fluence for 6 irradiated chip is shown in Fig. 4.6. As mentioned before, due to non-uniform beam distribution across the hybrid different chips have been irradiated to different fluences, however, we see consistent behaviour for all 6 chips. Furthermore, increase of noise is very close to this observed in the proton and in neutron irradiations.

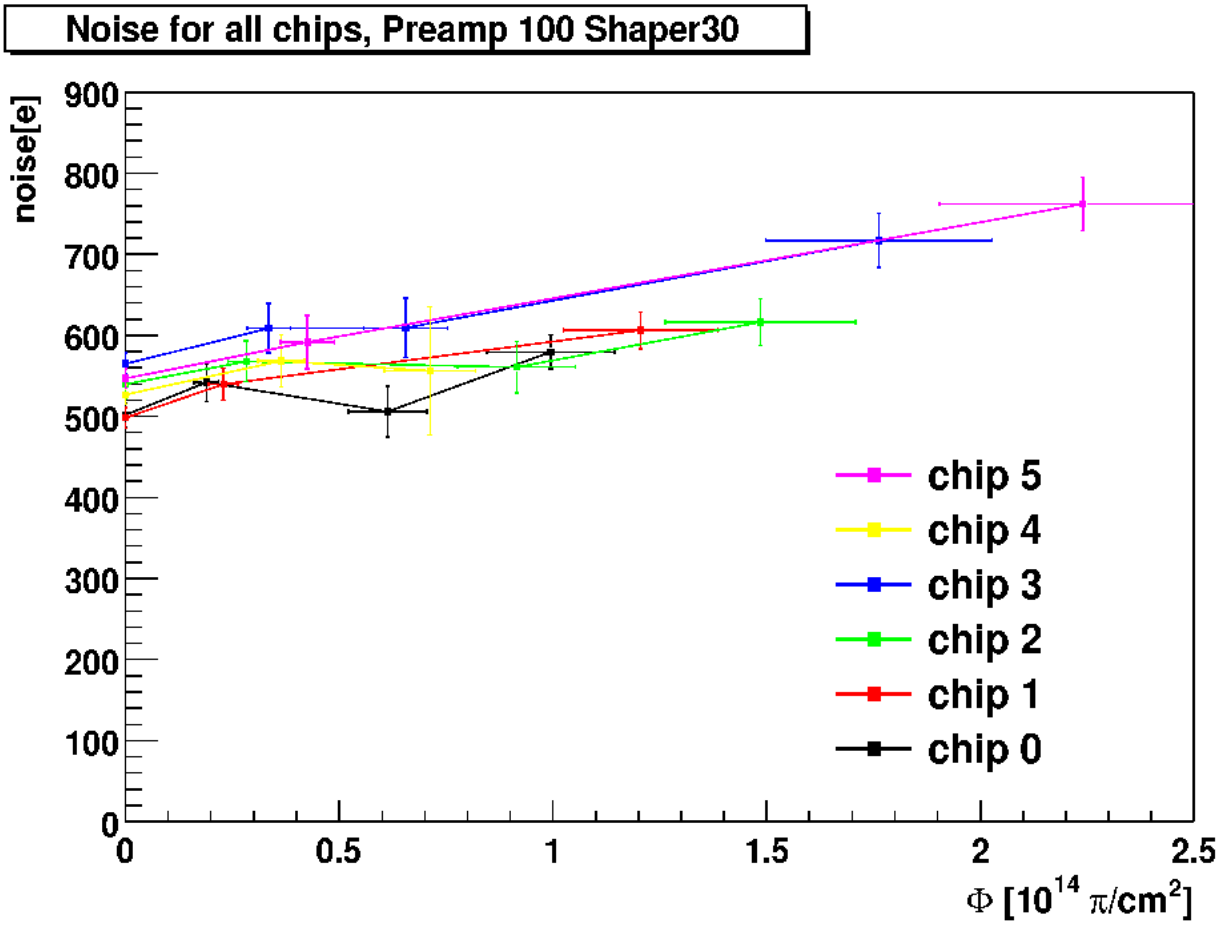

Figure 4.6: Parallel noise as a function of pion fluence.

Evolution of the offset spread vs pion fluence for 6 irradiated chips is shown in Fig. 4.7. The behaviour is very similar to this observed in proton irradiation, i.e. a rapid increase at the beginning and saturation at a level about 3-4 with respect to the pre-rad value.

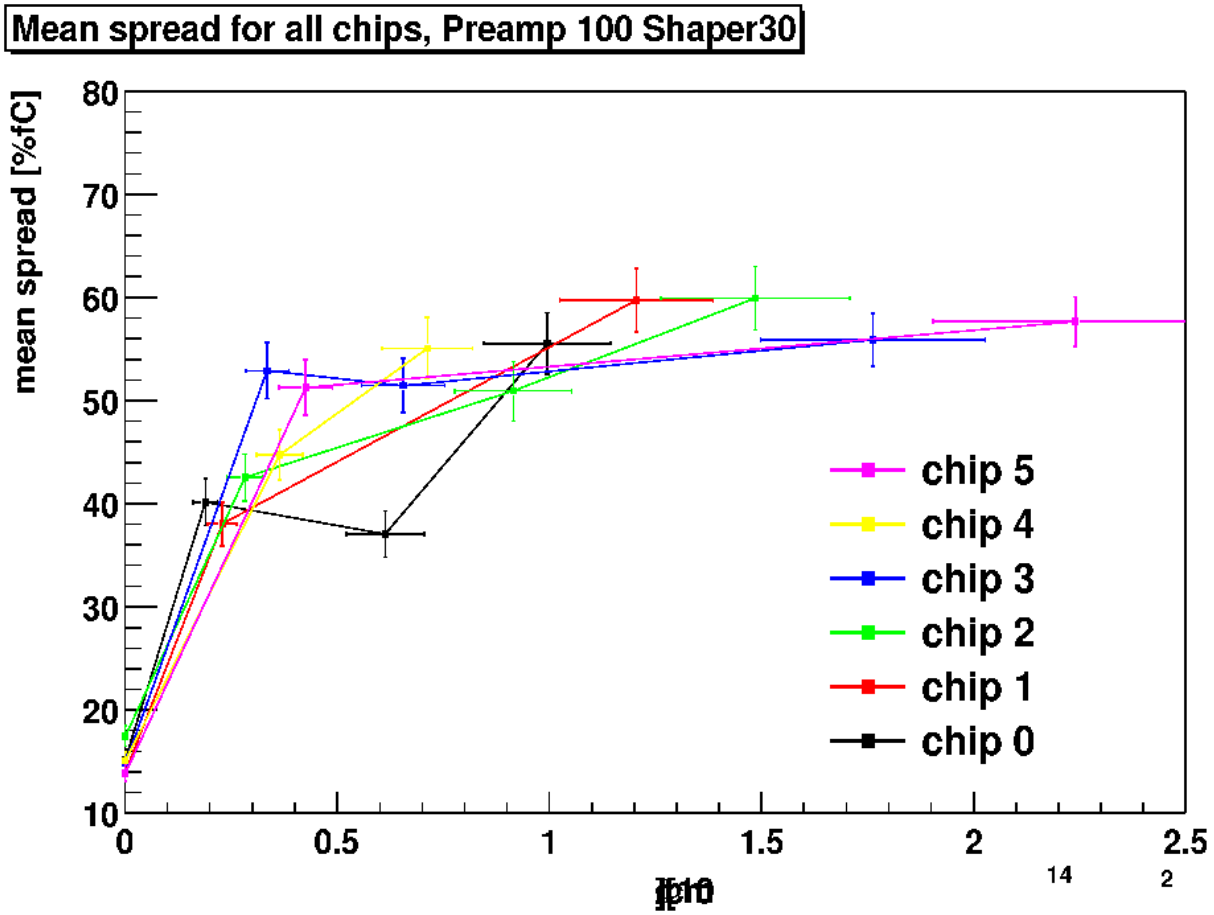

Figure 4.7: Evolution of offset spread as a function of pion fluence.

From the presented results one can draw a conclusion that pion irradiation does not introduce any unexpected effect. Degradation of analogue parameters is the analogue parameters consistent with this observed in proton and in neutron irradiations given the amount of TID and NIEL delivered to the chips.

4.3.2.3 SINGLE EVENT EFFECTS

Similar note as made with respect to analogue performance applies to the SEE measurements. Namely, the design of the pipeline and all static registers has not been change between the ABCD2T and ABCD3TA version. Therefore, the SEE sensitivity measured on the ABCD2T chips can be applied to the pipeline and all static registers in the ABCD3TA version.

Given a different time structure of the pion beam at PSI compared to the proton beam a modified data acquisition program was run to measure the chip sensitivity to SEE. As in the proton irradiation the SEE sensitivity was measured for the pipeline and for the mask register. Summarised results of this test are shown in Table 4.5. The sensitivity of the pipeline is on average by a factor 2.5 higher compared to proton irradiation while sensitivity of the mask register is on average lower by a factor 1.25 compared to proton irradiation. Given, however, limited precision of these measurements one can conclude the results from pion irradiation are consistent with the results from proton irradiation, as one can expect assuming that for the DMILL process the energy transfer threshold for SEE is well below 200 MeV.

Table 4.5: SEE rate in the pipeline and the mask register measured in 24 GeV/c proton beam at PS.

Chip position on hybrid	M0	S1	S2	S3	S4	E5	
SEE in pipeline	2.67	2.66	3.38	2.78	2.62	2.83	$\times 10^{12}/\pi/cm^2/flip$
SEE in static registers	5.29	4.14	3.19	3.17	3.08	2.89	$\times 10^{13}/\pi/cm^2/flip$

4.4 X-RAY IRRADIATION

X-ray irradiation has been performed for single chips mounted on dedicated test boards. Main goal of this irradiation was to study in detail the effect of the total ionising dose on the digital part of the ABCD3TA design. The irradiation was performed using CERN X-ray facility. The tube power supply is adjustable from 20 to 60 keV and has a beam diameter up to 1cm with the possibility to focus the beam down to a spot of 100 μm. There are two target materials: W (peak 10 keV) and Mo (peak 19 keV). Dose rate can be adjusted between 10 and 800 rad/s (48krad/min).

During irradiation the chips were connected to the SCT readout system so that they were irradiated in the nominal operating conditions. Testing was performed using an IC tester which allowed to test more details of the internal digital blocks and make a direct comparison with simulation. We expected that the speed of CMOS blocks will degrade after irradiation and sufficient speed margin has been included in the design. Since the speed of the CMOS circuits depends on the power supply there are two parameters which provide information about the speed margins of digital blocks:

- maximum speed measured at the nominal supply voltage of 4 V,
- minimum supply voltage at which the chip works correctly at 40 MHz.

Figure 4.8 shows degradation of speed of the ABCD2T chip after X-ray irradiation up to a total dose of 100 kGy. The results are shown for the most critical digital tests: TEST 1 - L1/BC counters check, TEST 2 - configuration check, TEST 3 - L1 overflow check, TEST 4 - data taking. We observe a degradation of speed almost by a factor of 2, nevertheless, after 100 kGy the chips still meet the requirement of 40 MHz at the nominal supply voltage.

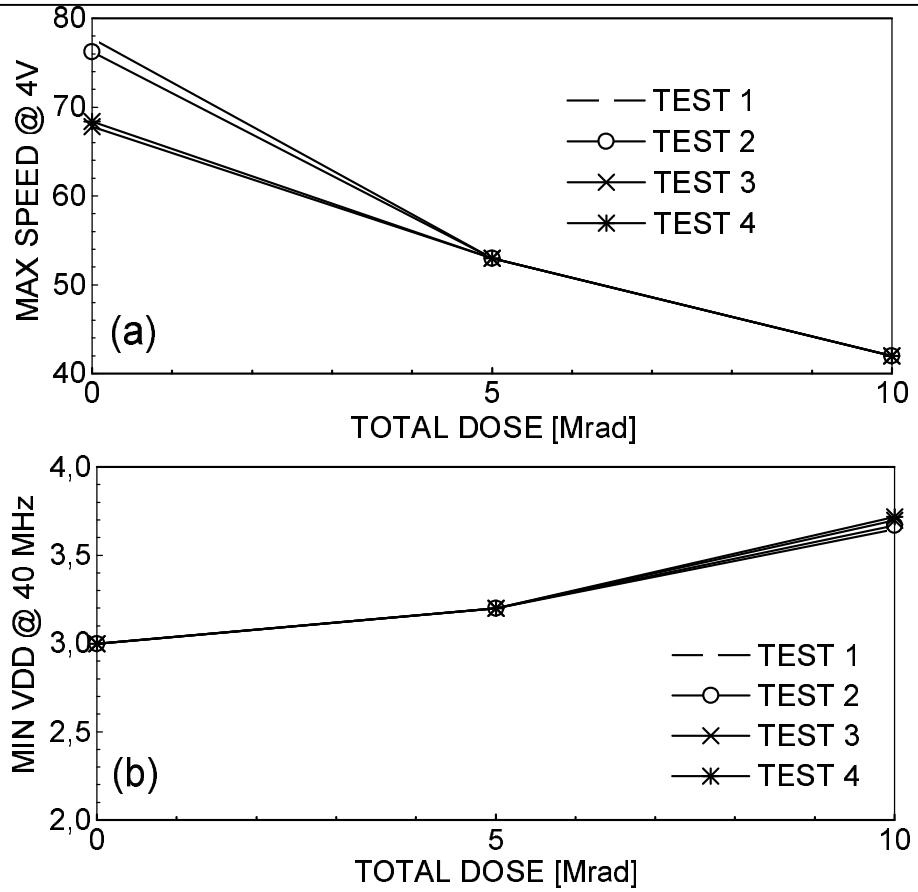

Figure 4.8: Maximum speed at supply voltage of 4 V (a) and minimum supply voltage at 40 MHz, (b) as a function of total ionising dose.

In the ABCD3TA design further tunning of signal timing between various digital blocks has been implemented in order to increase the speed even more in order to account for additional process variation. Typical degradation of the maximum clock frequency vs. total ionising dose for ABCD3T chip is shown in Fig. 4.9. Since the test was done with a high dose rate the standard high temperature annealing was performed in order to simulate irradiation with a low dose rate. After full dose of 10 Mrad the maximum clock frequency is 52 MHz at nominal supply voltage of 4 V has been achieved, compared to the required 40 MHz.

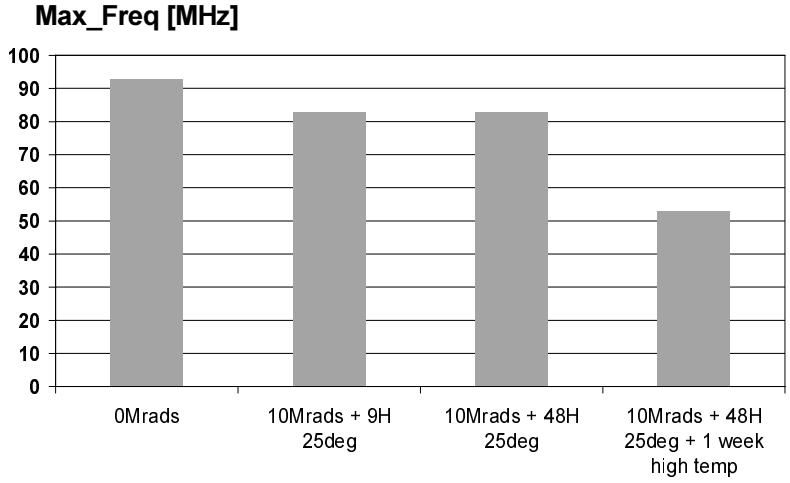

Figure 4.9: Evolution of the maximum cock frequency after irradiation and annealing.

Using X-rays we have investigated the effect of the leakage current which appears in the digital part of the chip after ionising irradiation. This effect was observed at various levels in the PS irradiations and it always showed some annealing, however, for the hybrids or full modules we could not perform a systematic study of high temperature annealing as foreseen for CMOS circuit after high dose rate irradiation. The result of a dedicated test performed using the X-ray is summarised in Fig. 4.10. The plot shows the digital supply current before irradiation, immediately after irradiation and evolution in time when performing high temperature annealing. At high temperature the excessive current anneals very quickly down to a level, which is close the initial value.

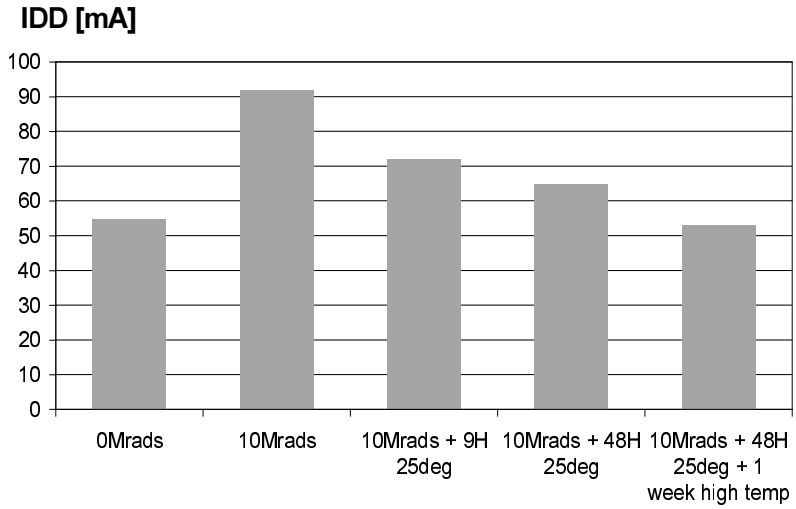

Figure 4.10: Evolution of the digital supply current after irradiation and annealing.

4.5 LOW DOSE RATE EFFECT STUDY

Since the ABCD3TA design uses extensively bipolar transistors in the analogue part we have performed a dedicated experiment to study the low dose rate effects in the DMILL technology. The irradiation of bipolar transistors with different dose rates have been performed using Co-60 sources. In addition irradiation at high dose rates and elevated temperature were performed.

Figure 4.11 shows the relative change of current gain factor β in bipolar transistors as a function of dose rate for the total ionising dose of 1.2 Mrad. The plot does not indicate any significant low dose rate effect.

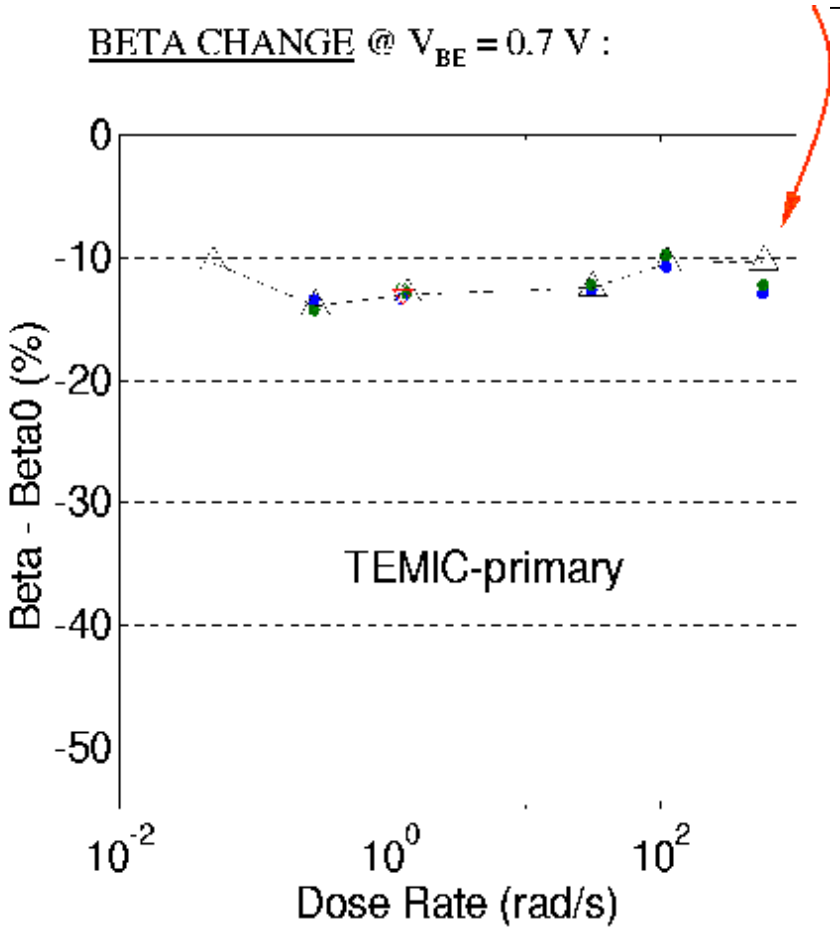

Figure 4.11: Beta of bipolar transistors as a function of dose rate for a total dose of 1.2 Mrad.

With the lowest dose rate of 0.05 rad/s we have reached the total dose of 1.2 Mrad. For higher dose rates we have irradiated the transistors to a full dose of 10 Mrad. Combined plot including all irradiations is shown in Fig. 4.12. The plot confirms that degradation of β does not depend on the dose rate.

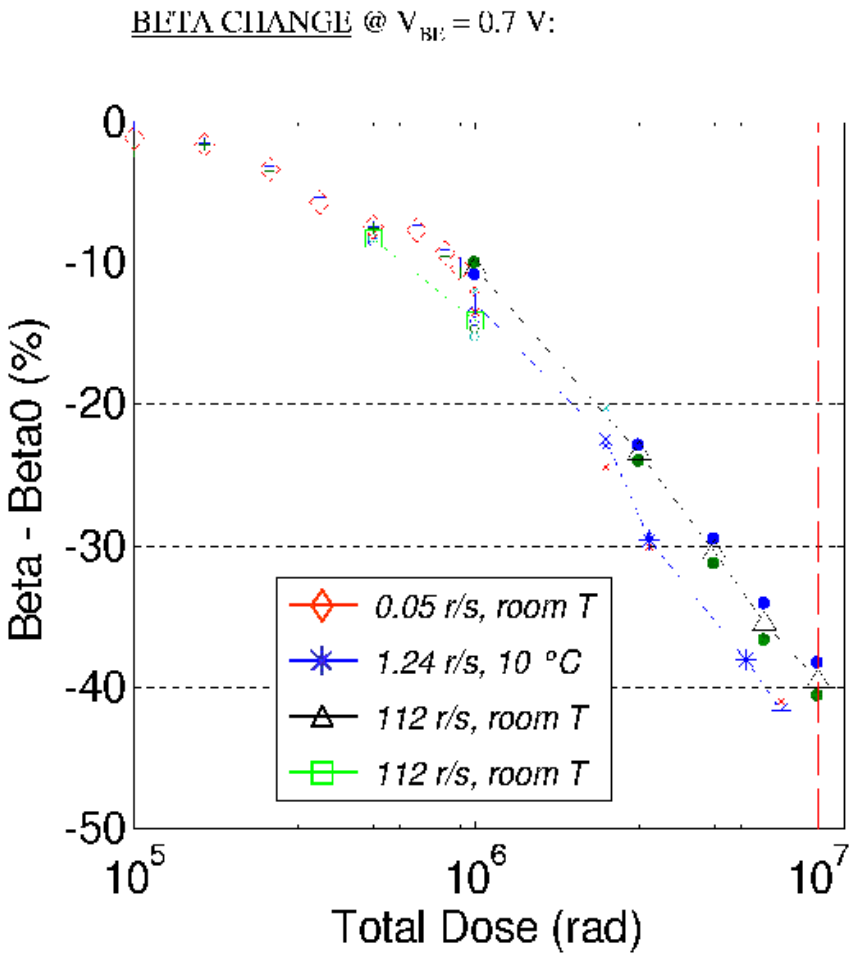

Figure 4.12: Degradation of β vs total dose for different dose rates.

5 SUMMARY

Extensive irradiation tests for large number of ABCD3TA ASICs for readout of silicon strip detectors confirm satisfactory radiation resistance of the ABCD3TA design up to the nominal radiation levels as specified in the ATLAS Inner Detector TDR.